

CBCS SCHEME

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18CS34

Third Semester B.E. Degree Examination, Jan./Feb. 2021 Computer organization

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. How to measure the performance of a computer? Explain. (08 Marks)
b. Define addressing modes. Explain any five types of addressing modes with example. (12 Marks)

OR

- 2 a. Define subroutine and parameter passing. Explain how to pass the parameter by value and by reference. (10 Marks)
b. How the input and output operations are to be performed by the processor? Write a program that reads a line of characters and displays it. (10 Marks)

Module-2

- 3 a. Write the scenario when the interrupts are enabled. (06 Marks)
b. Explain how the I/O devices should be organized in a priority structure. (08 Marks)
c. Define exception, describe the different kinds of exceptions. (06 Marks)

OR

- 4 a. Define bus arbitration. Explain the two approaches to bus arbitration. (10 Marks)
b. With the help of timing diagram, explain the read operation on the PCI bus. (10 Marks)

Module-3

- 5 a. Explain the operation of a CMOS memory cell. (06 Marks)
b. With a neat figure, explain the organization of a $2M \times 32$ memory module using $512K \times 8$ static memory chips. (08 Marks)
c. Explain the internal structure of synchronous DRAM. (06 Marks)

OR

- 6 a. What is the use of a cache memory? Explain in detail the three types of determining the cache locations to store memory blocks. (10 Marks)
b. How the parallelism is to be used as on interleaving? Explain. (10 Marks)

Module-4

- 7 a. A half adder is a combinational logic circuit that has two inputs x and y and two outputs sum(s) and carry(c), resulting from the binary addition of x and y .
i) Design a half adder as a two-level AND-OR circuit.
ii) Show how to implement a full-adder using two half address and external logic gates, as necessary. (10 Marks)
b. Given, multiplicand $A = +23$ and multiplier $B = -10$. Perform the multiplication of A and B using Booth's algorithm. (10 Marks)

Important Note : 1. On completing your answers, comp...only draw diagonal cross lines on the remaining blank page...
2. Any revealing of identification, appeal to evaluator and /or equations written eg, $42+8=50$, will be treated as malpractice.

OR

- 8 a. Explain 4-bit carry-look ahead adder. (10 Marks)
- b. Perform the division of $8 \div 3$ using restoring division. (10 Marks)

Module-5

- 9 a. Write and explain the control sequence for execution of the instruction Add(R3), R1. (10 Marks)
- b. Explain the three-bus organization of the data path. (10 Marks)

OR

- 10 a. Explain in detail the organization of control unit. (10 Marks)
- b. Explain the operation of 4-stage pipeline. (10 Marks)
